Research and Development Lixia Tang

ECN#

362

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_fwirlight

ENGINEERING CHANGE NOTE:



ECN#: 3

ASSEMBLY:	BMW4011		DESCRIPTION: PXY CPU CARD		CPU CARD				
New Assembly:	\mathbf{y} :		DATE: 25/0		25/05	/05/00			
Current Assy Rev:	Н	Н	Current Schematic Re	ev:	4.6	5.3			
New Assy Rev:	J	J	New Schematic Re	v :	4.7	5.4			
CMS BOMs Update	ed •	Excel BOMs Updated	Subcontractor Records	s Upda	ated	Compatibility Maintained:	Yes		
IMPLEMENTATION INFORMATION:									
Safety Issue	\circ	UL Compliance Issue	O New Feature		\bigcirc	Cost Reduction			
Bug Fix	\circ	EMC Compliance Issue	Ouality Issue						

○ Cosmetic Change

REASON FOR CHANGE:

Reliability Reasons

Adjust main clocking crystal for SIO1 timing.

DETAILS OF CHANGE:

1. Change X1 to 14.32MHz 10ppm. Fairlight P/N XMD5980

Software Change

2. Place revision resistors (all 10k SMD0603 Fairlight P/N RMD8573) as follows:

For Rev 4 PCBs			For Rev 5 PCBs				
	10k	Omit		10k	Omit		
-							
R127		X	R127	X			
R128	X		R128		X		
R133		X	R133	X			
R134	X		R134		X		
D125		v	D125		v		
R135		X	R135		X		
R137	X		R137	X			
R136	X		R136	X			
R138		X	R138		X		

^{3.} Place a assembly revision label on the card, marked "J", after the blank PCB P/N so it reads as follows: BMW4011D-J (Rev 4 boards) or BMW4011E-J (Rev 5 boards)